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A HIGH SPEED FFT/IFFT PROCESSOR FOR MIMO OFDM SYSTEMS

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Abstract*— A Novel super-pipelined Architecture including viterbi algorithm for implementation of fast fourier transform (FFT) Processors for multiple-input multiple-output Orthogonal frequency division multiplexing (MIMO-OFDM) systems. The super pipelined architecture is capable of achieving high throughput in an area efficient manner. A pipelined architecture is proposed to realize the Viterbi algorithm for moderate speed applications. This architecture can effectively reduce the silicon area necessary for the VLSI implementation of the Viterbi algorithm with the large constraint length. The existing system is a variable length FFT processor for MIMO-OFDM based SDR systems in which butterfly diagram is used in every stage of internal processing. So it will increase the processing time at result it will reduce the speed and take memory to store the each value in butterfly process. Finally it increases the memory size. It consists of only pipelined architectures. A reduced memory FFT Processor can be implemented by using a Multi path delay commutator (MDC) based architecture. Only one MDC is used in the system and it will be available to every stage, so that the complexity and memory usage can be reduced. The MDC based system is efficient in terms of area but it is not efficient in terms of power. For the speed improvement we are proposing a new system with viterbi algorithm inside the FFT rather than the radix-2 algorithm. It can be applied to various wireless communication applications. The processor was implemented with an UMC90-nm CMOS technology. We are implementing the FFT processor with radix -2 algorithms that includes only one MDC for reducing the memory. A super- pipelined architecture based FFT processor for moderate speed application with reduced memory is proposed. An ACS (adds, compare and select) unit for the viterbi decoder with the constraint length 7 is designed to demonstrate the feasibility of this architecture in a 0.6 µm 3.3V triple-metal CMOS process.

Keywords*— Fast fourier transform(FFT); Multiple-input multiple-output(MIMO); Orthogonal frequency division multiplexing(OFDM); Multi path delay commutator(MDC).

I. INTRODUCTION

In recent years, multiple-input multiple-output (MIMO) transmission technology has been widely applied to various wireless communication systems.

Digital communication using MIMO has been regarded as one of the most significant technical breakthrough modern communications. MIMO technology is divided into three categories, precoding, spatial multiplexing and diversity coding. Precoding is a generalization of beam forming to support multi-layer transmission in multi-antenna wireless communications. In conventional single-layer beam forming, the same signal is emitted from each of the transmit antennas with appropriate weighting such that the signal power is maximized at the receiver output. When the receiver has multiple antennas, single-layer beam forming cannot simultaneously maximize the signal level at all of the receive antennas. Thus, in order to maximize the throughput in multiple receive antenna systems, multi-layer beam forming is required.

In the spatial multiplexing technique, the data is split into multiple streams, which are transmitted and received by multiple antennas. Subsequently, the receiver detects the transmitted symbols from the signals received by the multiple receiving antennas. In addition, the diversity coding technique has a better capability of resisting the channel impairment. The most popular diversity coding technique is space-time coding (STC) which involves space diversity, modulation, and error correction. The STC can moderately improve the spectral efficiency and provide coding gains for error correction.

In many areas of digital signal and image processing there is a need to reorganize sequences of digital data between the computational processing stages of a digital processing system. One particularly important area is in the computation of fast Fourier transforms. The fast Fourier transform (FFT) is well known mathematical algorithms for performing Fourier transform operations. The Fourier transform is widely used in Digital Signal Processing (DSP) applications to determine the frequency spectral content of digital signals or data. Simply the terms FFT and IFFT are used to denote efficient and fast algorithms to compute the Discrete Fourier Transform (DFT) and the Inverse Discrete Fourier Transform (IDFT)

respectively. The mathematical operations, including the FFT, are often implemented in hardware. When so implemented, the data reorganization is commonly effected using a commutator circuit. Existing commutator circuits are, however, application specific. For example, in the case of an FFT processor, which would comprise a number of commutator circuits, each commutator circuit is individually devised according to a There are a considerable number of known algorithms which may be used to implement any particular FFT and the structure of the commutator circuit is also dependent on which algorithm is used for the application in question.

It will be appreciated therefore, that there are a considerable number of permutations of factors which determine the structure of the commutator circuit. Conventionally, once a commutator circuit is designed in accordance with a particular combination of application requirements, the circuit is dedicated for use with that particular combination of requirements. The design of commutator circuits for an FFT processor by conventional methods is a labor intensive procedure, typically requiring months of design time. The FFT/IFFT is widely used in many digital signal processing applications and the efficient implementation of the FFT/IFFT is a topic of continuous research.

With the development of digital communications, high speed large-constraint-length Viterbi decoders will be required to yield higher coding gain and provide large ability to transmit more data in the same channel. An efficient trade-off between area and speed has to be done in VLSI implementation of high speed large-constraint-length Viterbi decoders. To date, the pipelined architecture is one of the best choices for high throughput and large-constraint-length Viterbi decoders.

The hardware implementation of Viterbi algorithm mainly includes two processes: one is the ACS (add, compare and select) process and another is the traceback process. Generally, the ACS unit dominates the silicon area of the Viterbi decoder. When the constraint length is large, an area-efficient ACS is a major impediment to VLSI single-chip implementation of the Viterbi algorithm. To date, the Viterbi decoders with constraint length 9 or higher are required in some communication systems.

In this case we propose a new pipelined architecture including viterbi algorithm within the FFT processor for moderate speed applications in wireless communications. There are several structural similarity between the FFT algorithm and viterbi algorithm. Their basic process element is a butterfly. The two number of application requirements such as: the size of the transform; the data word-lengths; the data word-widths; and the level of pipelining in the FFT processor. The transform size relates to the number of data samples in one data block, or data set, and is commonly expressed as the 'point' of the transform. Furthermore,

algorithms have the same memory management and computation process.

The fig.1 shows the block diagram for the implementation of FFT processor with radix-2 algorithm within it the input signal will be a serial one. It can be converted into parallel. The FFT/IFFT processer will get multipath input. FFT/IFFT will perform the radix -2 algorithm in pipelined architecture. Then the commutator will use the butterfly diagram as once in a stage. it will utilise it to all stages. FFT/IFFT produces the multipath output. This will be converted into serial by using parallel to serial converter. it produces the serial output at the receiver end. Serial to parallel converter is somewhat the reverse operation of parallel to serial converter. It is a circuit for converting a serial data input stream to parallel data. Shift registers are used for the conversion between Serial and Parallel formats. Once the input data is given, it may be either read off at each output simultaneously, or it can be shifted out and replaced. Parallel to serial converter is a circuit for converting a parallel data input stream to serial data. This configuration has the data input on lines D1 through D4 in parallel format. To write the data to the register, the Write/Shift control line must be held LOW. To shift the data, the W/S control line is brought HIGH and the registers are clocked.

In communication we sent data serially, that is bi by bit. But If we are using an FFT/IFFT processor, they need a number of inputs at the same time. So we convert the serial signal into parallel by using a converter and then feed into an FFT/IFFT.

II. FFT ALGORITHM

The FFT is a fast algorithm for computing the DFT. If we take the 2-point DFT and 4-point DFT and generalize them to 8-point, 16-point,...,2*r*-point, we get the FFT algoritham.There are many variants of the FFT algorithm such as decimation in Time FFT algorithm and decimation in frequency FFT algorithm.

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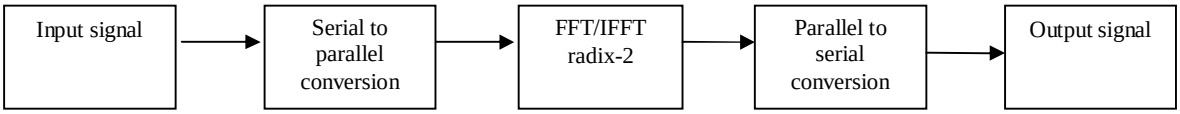

Fig.1: Block diagram for the implementation of FFT processor with radix-2 algorithm

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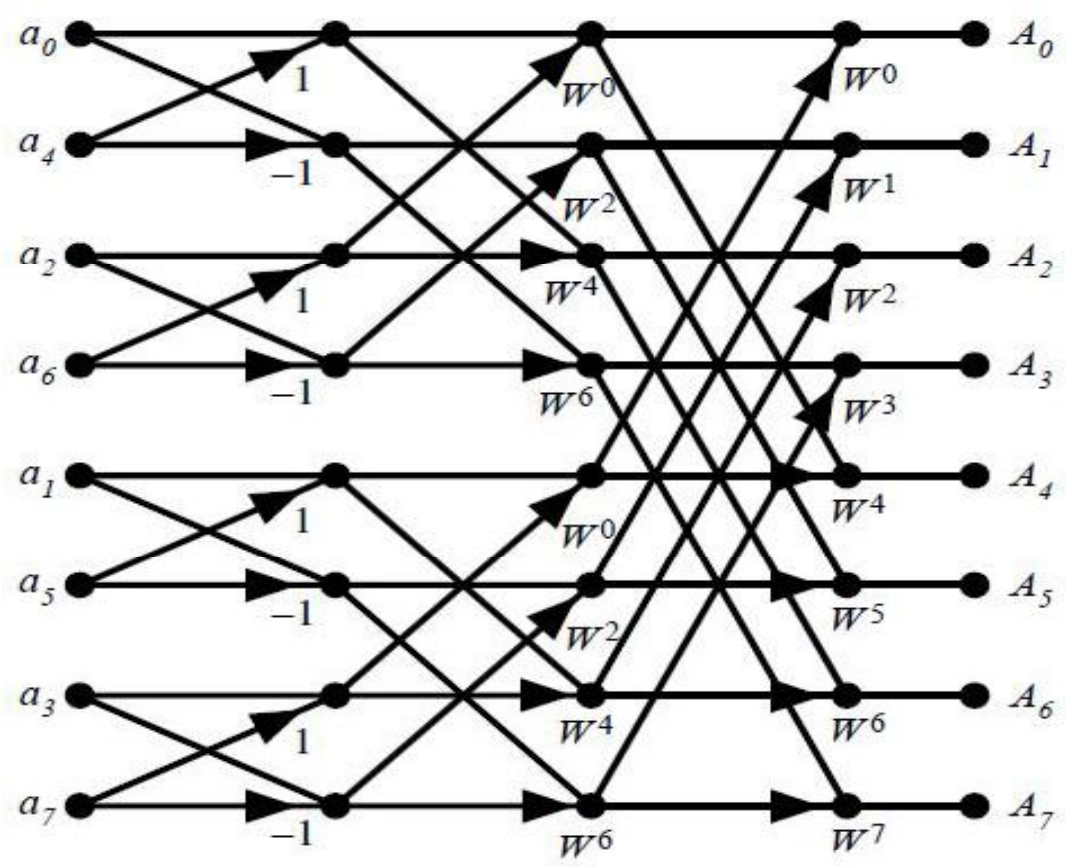

Fig 2 : Eight point FFT

2.1 Butterflies and Bit-Reversal

The FFT algorithm decomposes the DFT into $\log_2 N$ stages, each of which consists of N=2 butterfly computations. Each butterfly takes two complex numbers p and q and computes from them two other numbers. Fig 3 is a diagram of a butterfly operation.

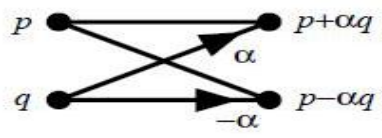

Fig 3 Butterfly Operation

The butterfly operation consists of addition and subtraction operation.

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2.2 Radix-4 FFT algorithm

In order to improve the power reduction, we propose a radix-4 64-point pipeline FFT/IFFT processor. In order to speed up the FFT computations, more advanced solutions have been proposed using an increase of the radix. The traditional FFT algorithms of radix 2 type have simple structure and data flow, which are easy to implement and are suitable for generic FFT implementation. These algorithms need large memory to store data at inner stages, which require large power and area consumption.

The radix-4 FFT algorithm is most popular and has the potential to satisfy the current need. The radix-4 FFT equation essentially combines two stages of a radix-2 FFT into one, so that half as many stages are required. To calculate 16-point FFT, the radix-2 takes $\log_2 16=4$ stages but the radix-4 takes only $\log_4 16=2$stages. A 16-point, radix-4 decimation-in-frequency FFT algorithm is shown in Fig 4. Its input is in normal order and its output is in digit-reversed order. It has exactly the same computational complexity as the decimation-in-time radix-4 FFT algorithm.

Fig.4 shows a 16-point radix-4 decimation-in-frequency FFT algorithm

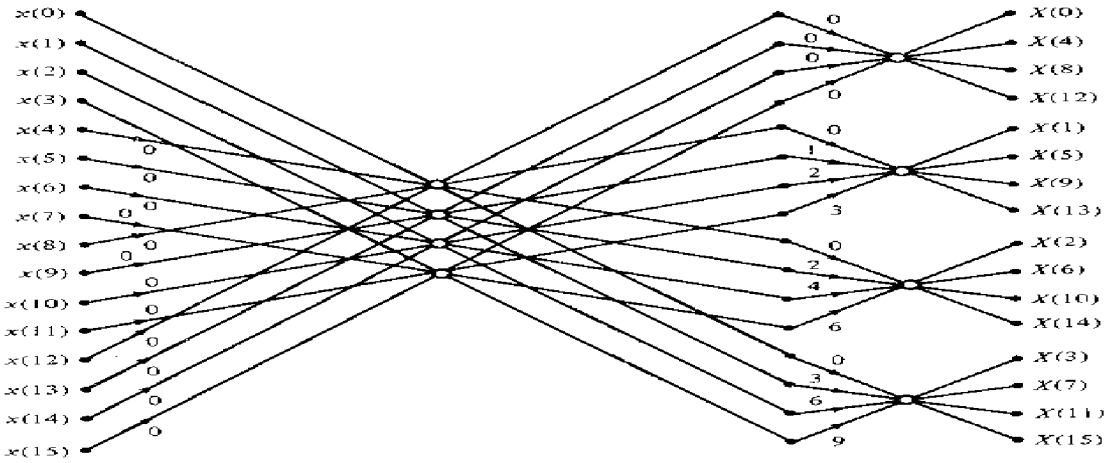

Fig 4: A 16-point radix-4 decimation-in-frequency FFT algorithm

When the number of data points N in the DFT is a power of 4, then is more efficient computationally to employ a radix-4 algorithm instead of radix-2 algorithm. A radix-4 decimation in-time FFT algorithm is obtained by splitting the N-point input sequence x(n)into four sub sequences x(4n), x(4n + 1), x(4n + 2) and x(4n + 3). Its input is in normal order and its output is in digit-reversed order. It has exactly the same computational complexity as the decimation-in-time radix-4 FFT algorithm. A 16-point, radix-4 decimation-in-frequency FFT algorithm is shown in Figure.1 the radix-4 decimation in frequency butterfly is constructed by merging 4-point DFT with associated coefficients between DFT stages.

A N-point DFT is defined as

$X[K]=\sum_{n=0}^{N-1} x[n]w^{nk}$,k=0,1,2,……..N-1;

Where,$W^{nk}=e^{-j2\pi nk/N}$

2.3 Viterbi Algorithm

Viterbi algorithm is based on dynamic programming computations. Its data flow can be expressed by a trellis graph. The vertices of trellis are called *states* and associated numerical values path metric *pm*. When the constraint length is *v*, the trellis graph contains 2^{v-1}states at any given time. Edge weights are given by the branch metric *bm*. One of the major steps in the Viterbi algorithm is to update the path metrics.

Fig.5 shows this updating process. Every new path metric is the lesser of two sums, which is old path metric plus its corresponding branch metric. So we call it add, compare and select (ACS) process.

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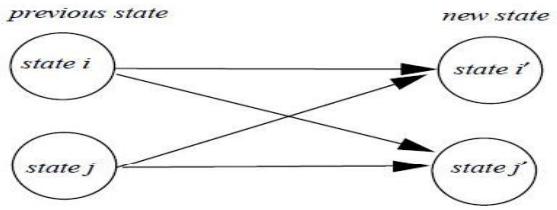

Fig 5 : A butterfly of updated path metric

2.4 Pipelined Architecture

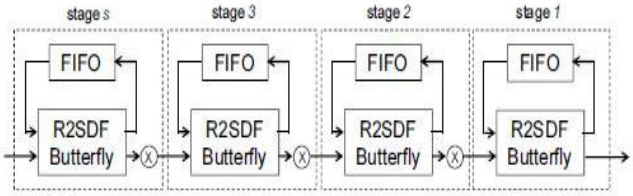

Fig 6 : Pipelined FFT architecture

ACS is based on the radix-2 SDF architecture which utilizes memory much more effectively. Only one RAM is required. Fig.4.2 shows its architecture for a 16-point DIF FFT, where the data is processed between stages in a single path and feedback is used to store new inputs and intermediate results.

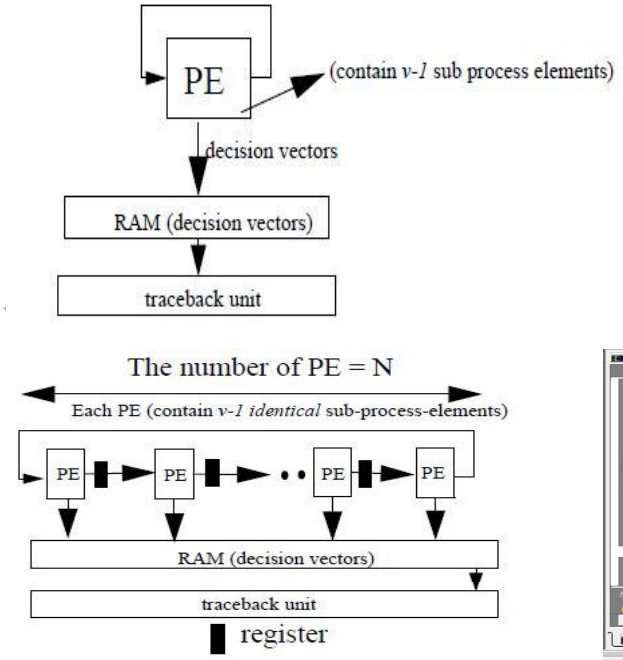

Fig 8: super-pipelined architecture

In last three decades, various FFT architectures such as single-memory architecture, dual memory architecture, pipelined architecture, array architecture and cache memory architecture have been proposed. Pipeline architectures are well suited to achieve Small silicon area, High throughput, short processing time and reduced power consumption. Several pipelined architectures have been developed to realize FFT algorithm, such as Multi-path Delay Commutator (MDC), Single-Path Delay Feedback (SDF) and single-path Delay Commutators.

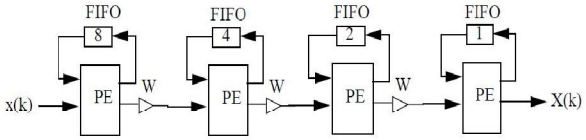

Fig 7 : Radix-2 SDF architecture for a 16-point FFT

III. SUPER-PIPELINED VITERBI ARCHITECTURE

PE (one full in-place computation cycle) is the basic unit of the Viterbi decoder. Inside each PE, the pipelined architecture has been used to cascade the sub-process-element. Figure 5.1.shows the simplified SDF pipelined architecture for Viterbi decoders (constraint length is 10) where only one computation cycle (PE) is utilized. In order to further increase the speed, the PE can be further cascaded and pipelined which is called "super-pipelined architecture". Fig 8. shows this super-pipelined architecture where N process elements (PE) are pipelined. The speed will be linearly increased by the factor of N (the number of PE).Meanwhile this architecture do not increase the control complexity significantly which can be efficiently implemented in VLSI.

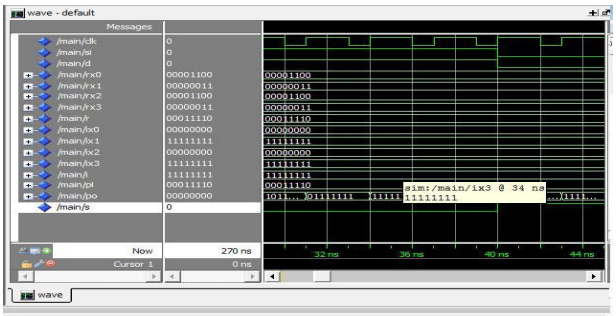

Fig 9: Simulation result of the FFT processor with radix-2 algorithm

The input data is given to the serial to parallel converter. clk, si and d are the inputs. r is the real part and i is the imaginary part of the butterfly operation.
r=rx0+rx1+rx2+rx3
i=ix0+ix1+ix2+ix3
s is the FFT output.

In Fig.5.2, each PE (process element) includes four adders and two comparators and four multiplexers. After 4 stages inplace computation, the path metric restores to natural order. And then natural order path metrics can be send to ACS to update the old path metric and another computation cycle is started again.

IV. SIMULATION RESULT

The fig 9. Shows the simulation result of the reduced memory FFT processor with radix-2 algorithm with one MDC. The input signal will be a serial one. That has to be converted into parallel by using a serial to parallel converter. The multiple outputs from serial to parallel converter is given to the FFT processor that will perform radix-2 algorithm. The output from the processor is passed through a parallel to serial converter and a serial output is obtained.

V. CONCLUSION

The new algorithm proposed a radix-r based MDC MIMO FFT/IFFT processor for processing Ns streams of parallel inputs, where r = Ns for achieving a 100% utilization rate. The proposed approach is suitable for MIMO-OFDM baseband processor such as WiMAX or LTE applications.we proposed an efficient memory scheduling to fully utilize memory. This considerably decreases the chip area because the memory requirement usually dominates the chip area in an FFT/IFFT processor. The reduction in memory usage also leads to effective power applications. There are structural similarity between FFT and Viterbi algorithm. Because both of the two algorithms are butterfly structures, the architectures developed for the FFT are appropriate for the viterbi algorithm as well. And then a pipelined architecture with viterbi algorithm inside the FFT is proposed for moderate architecture - Radix-2 SDF architecture was proposed, which can reduce the silicon area of Viterbi decoders dramatically. saving, which is important for mobile devices. The proposed designs found a good balance among. complexity, energy consumption, and chip area, for the MIMO-OFDM systems. An area efficient VLSI Speed

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